# EXHIBIT D

**IN THE UNITED STATES DISTRICT COURT**

**FOR THE DISTRICT OF DELAWARE**

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| S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES S.A. and SOITEC USA, INC.,<br><br>Plaintiffs and Counterclaim Defendants,<br><br>v.<br><br>MEMC ELECTRONIC MATERIALS, INC.,<br><br>Defendant and Counterclaim Plaintiff. | Civil Action No.: 1:05-cv-00806-*** |

**SUPPLEMENTAL AND AMENDED RESPONSE TO MEMC'S FIRST SET OF INTERROGATORIES (NOS. 1-31)**

Pursuant to Federal Rules of Procedure 26(e) and 33, Plaintiffs and Counterclaim Defendants S.O.I.TEC Silicon on Insulator Technologies S.A. and Soitec USA, Inc. (collectively, "Soitec") supplement and amend their prior response to the first set of interrogatories propounded by Defendant and Counterclaim Plaintiff MEMC Electronic Materials, Inc. ("MEMC") as follows.

**General Objections**

Soitec objects to MEMC's First Set of Interrogatories, and the definitions and instructions thereto, to the extent they:

1. Seek information, documents or things protected by attorney-client privilege, work product immunity, or any other privilege or immunity, or are otherwise protected from disclosure by law or by confidentiality obligations to third parties.

2. Attempt to impose obligations on Soitec that differ from, exceed, or conflict with those imposed under the Federal Rules of Civil Procedure and the Local Rules.

3. Purport to define a word or phrase as used in any of the claims of the patent-in-suit.

4. Attempt to define "Soitec," "Plaintiffs," or "Counterclaim Defendants" as encompassing any entity or person other than the Plaintiffs.

5. Seek information or the identity of documents not reasonably calculated to lead to the discovery of admissible evidence.

6. Require Soitec to provide response prior to its receiving MEMC's document production and substantive interrogatory responses.

7. Exceed the number of interrogatories allowed under Local Rule 26.1(b).

Soitec specifically incorporates each of these General Objections into its specific responses to each of MEMC's interrogatories, whether or not each such General Objection is expressly referred to in Soitec's response to a specific interrogatory.

To the extent a response is provided pursuant to Fed. R. Civ. P. 33(d) by reference to documents being produced, Soitec incorporates by reference herein its objections to MEMC's First Request for Production. Further, where such responses are given pursuant to Fed. R. Civ. P. 33(d), Soitec incorporates by reference correspondence from its counsel to counsel for MEMC identifying such documents, deposition testimony of its witnesses and experts identifying and/or explaining such documents, deposition testimony of its witnesses designated under Fed. R. Civ. P. 30(b)(6) to testify regarding topics responsive to these interrogatories, and the reports, declarations, and deposition or other testimony of its experts (when given).

Soitec reserves the right to assert additional or supplemental objections should Soitec discover additional grounds for such objections.

Soitec's investigations are ongoing and Soitec reserves the right to amend or supplement these responses.

**Responses**

**INTERROGATORY NO. 1: [Actual Interrogatory Nos. 1-3]**

Identify [1] each of your silicon on insulator products (including without limitation each Unibond product and [2] each product made using a "COP free" donor wafer for the device layer) by name and product number which was ever made, used, offered for sale, sold or shipped into the United States, and [3] identify the customer(s) for each of these products.

**RESPONSE:**

Soitec objects to this interrogatory to the extent that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence insofar as it concerns products that MEMC has not accused of infringement in this lawsuit. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Soitec also objects to the phrase "COP free" as vague and ambiguous.

Subject to and without waiving the foregoing specific and general objections, Soitec states that it has used four basic commercial processes ("POR," "P0," "P3," and "P5") to manufacture silicon on insulator products. Pursuant to Fed. R. Civ. P. 30(b)(6) and 33(d), Soitec has produced and will produce witnesses and has produced non-privileged documents from whom and from which MEMC can identify each of Soitec's silicon on insulator products made using a "COP free" (as best Soitec can understand that term) donor wafer for the device layer, and the customer(s) for each of these products.

**INTERROGATORY NO. 2: [Actual Interrogatory Nos. 4-6]**

For each Asserted Claim of the '104 patent, explain in detail the basis for Soitec's denial of infringement.

**RESPONSE:**

Soitec objects to this interrogatory to the extent it seeks information or documents protected by the attorney-client privilege or work product immunity. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Soitec objects that the interrogatory is also premature because MEMC has to date failed to provide Soitec with MEMC's proposed claim constructions and the Court has not yet construed the asserted claims. Soitec further objects to this interrogatory as premature to the extent it seeks expert opinion prior to any scheduled exchange of expert reports. Soitec further objects to this interrogatory as premature because MEMC has failed to provide Soitec with any information regarding the testing upon which MEMC purports to base its allegations of infringement

To the extent that Soitec understands this interrogatory and subject to and without waiving the foregoing specific and general objections, and subject to amendment and modification pursuant to Fed. R. Civ. P. 26, Soitec preliminarily states it does not infringe any of Claims 1, 9, or 10 because, to the extent that any claim of the '104 Patent is valid and enforceable, Soitec is entitled to practice it as a co-owner of the '104 Patent. Soitec further preliminarily states that it does not infringe any of Claims 1, 9, or 10 because those claims are invalid and unenforceable. Soitec further preliminarily states that it does not infringe any of Claims 1, 9, or 10 because MEMC cannot prove by a preponderance of the evidence that any accused product contains a device layer with a first axially symmetric region in which there is a predominant intrinsic point defect, which is substantially free of agglomerated intrinsic point

defects. This is true for at least the following reasons: During the process of fabricating Soitec's SOI products, the material constituting the device layer undergoes multiple processing steps which alter the defect structure of the starting material used to make the device layer. These steps include ion implantation, multiple oxidation steps and multiple anneals. It is Soitec's understanding that there is no known technique for determining whether the resulting device layer contains a first axially symmetric region in which there is a predominant intrinsic point defect which is substantially free of agglomerated intrinsic point defects, and no reason to believe that such a region exists.

Further, with respect to Claim 10, Soitec preliminarily states that MEMC cannot prove by a preponderance of the evidence that any accused product contains a device layer as set forth in Claim 1, wherein vacancies are the predominant intrinsic point defect, as discussed above with respect to claim 1.

**INTERROGATORY NO. 3: [Actual Interrogatory Nos. 7-8]**

State whether the device layer in any of the silicon on insulator products identified by Interrogatory Number 1, above, [1] contains any "agglomerated intrinsic point defects" as the quoted term is used in the Asserted Claims and, if so, explain in detail the factual basis for your belief that such defects are present and [2] identify all test results and documents which corroborate such belief.

**RESPONSE:**

Soitec objects to this interrogatory to the extent that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent it concerns products that MEMC has not accused of infringement in this lawsuit. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Soitec also objects that this interrogatory is vague and ambiguous to the extent it seeks an application of selected claim elements without providing MEMC's proposed construction of those elements.

Soitec also objects to MEMC's mischaracterization in this interrogatory of the scope and proper construction of the asserted claims in this lawsuit. Soitec further objects to this interrogatory as premature to the extent it seeks expert opinion prior to any scheduled exchange of expert reports. Soitec further objects to this interrogatory as premature because MEMC has failed to provide Soitec with any information regarding the testing upon which MEMC purports to base its allegations of infringement

To the extent that Soitec understands this interrogatory and subject to and without waiving the foregoing specific and general objections, and subject to amendment and modification pursuant to Fed. R. Civ. P. 26, Soitec preliminarily states it does not examine the device layers of its products to determine if the device layers contain "any 'agglomerated intrinsic point defects,'" it is not aware of any means for doing so, and it has no reason to believe that the device layers in its products lack agglomerated intrinsic point defects.

Further responding, Soitec notes that MEMC apparently is contending that the limitations of the asserted claims covering a "device layer. . . substantially free of agglomerated intrinsic point defects" should be interpreted to refer to any device layer made from material that originally was a part of a donor wafer wherein the donor wafer has the claimed properties, regardless of whether the device layer retains the claimed properties when made, used, sold, or offered for sale in the United States or imported into the United States as part of the claimed silicon on insulator structure. Soitec denies that this is the proper interpretation of this limitation. Using (without adopting) MEMC's incorrect construction of this limitation, Soitec states that it is in possession of, and has produced, documentation showing that at least some of its silicon on insulator products have device layers taken from starting material which contains "agglomerated intrinsic point defects." Further, Soitec is uncertain as to how to test to determine whether

"agglomerated intrinsic point defects" are "substantially absent" from a device layer as those terms are used in the asserted claims (however construed) and contends that there is no scientifically reliable method for doing so. In corroboration of this contention, Soitec relies, *inter alia*, on the Federal Circuit's decision in *MEMC Electronic Materials v. Mitsubishi Materials Silicon Corporation, et al.*, 2006-1306, 1326 (September 20, 2007); United States Patent No. 6,391,662; and the deposition testimony of Robert Falster, MEMC's corporate designee under Fed. R. Civ. P. 30(b)(6) and the sole named inventor on the '104 Patent. Soitec will further rely on the report or reports of one or more of its expert witnesses and the materials cited therein in corroboration of this contention. Such reports will be submitted in conformity with the Court's scheduling order.

**INTERROGATORY NO. 4: [Actual Interrogatory Nos. 9-10]**

State whether the device layer in any of the silicon on insulator products identified by Interrogatory Number 1, above, [1] contains a region substantially free of "agglomerated intrinsic point defects" as the quoted term is used in the Asserted Claims and, if so, explain in detail the factual basis for your belief that such defects are not present and [2] identify all test results and documents which corroborate such belief.

**RESPONSE:**

Soitec objects to this interrogatory to the extent that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent it concerns products that MEMC has not accused of infringement in this lawsuit. Soitec further objects to this interrogatory on the grounds that the size, location, and geometry are of the "region" in question are undefined and, as such, the interrogatory is unduly vague and cannot be responded to or, if construed to cover a "region" of any size, location, or geometry, Interrogatory No. 4 is duplicative of Interrogatory No. 3. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Soitec also objects that this interrogatory is

vague and ambiguous to the extent it seeks an application of selected claim elements without providing MEMC's proposed construction of those elements. Soitec also objects to MEMC's mischaracterization in this interrogatory of the scope and proper construction of the asserted claims in this lawsuit. Soitec further objects to this interrogatory as premature to the extent it seeks expert opinion prior to any scheduled exchange of expert reports.

To the extent that Soitec understands this interrogatory and subject to and without waiving the foregoing specific and general objections, and subject to amendment and modification pursuant to Fed. R. Civ. P. 26, Soitec preliminarily states that it does not examine the device layers of its products to determine if the device layers contains "a region substantially free of 'agglomerated intrinsic point defects'," is not aware of any means for doing so, and has no reason to believe that the device layers in its products are lacking in agglomerated intrinsic point defects.

Further responding, Soitec notes that MEMC appears to be contending that the limitations of the asserted claims covering a "device layer. . . substantially free of agglomerated intrinsic point defects" should be interpreted to refer to a device layer which originates as part of a donor wafer wherein the donor wafer has the claimed properties, regardless of whether the device layer retains the claimed properties when the SOI wafer is made, used, sold, or offered for sale in the United States or imported into the United States as part of the claimed silicon on insulator structure. Soitec denies that this is the proper interpretation of this limitation. Using (without adopting) MEMC's incorrect construction of this limitation, Soitec states that it is aware of, and has produced, documentation showing that at least some of its silicon on insulator products have device layers taken from starting material that does not have "a region [(to the extent understood)] substantially free of 'agglomerated intrinsic point defects.' " Further, Soitec

is uncertain as to how to test for "agglomerated intrinsic point defects" as that term is used in the asserted claims (however construed) and contends that there is no scientifically reliable method for doing so. In corroboration of this contention, Soitec relies, *inter alia*, on the Federal Circuit's decision in *MEMC Electronic Materials v. Mitsubishi Materials Silicon Corporation, et al.*, 2006-1306, 1326 (September 20, 2007); United States Patent No. 6,391,662; and the deposition testimony of Robert Falster, MEMC's corporate designee under Fed. R. Civ. P. 30(b)(6) and the sole named inventor on the '104 Patent. Soitec will further rely on the report or reports of one or more of its expert witnesses and the materials cited therein in corroboration of this contention. Such reports will be submitted in conformity with the Court's scheduling order..

**INTERROGATORY NO. 5: [Actual Interrogatory Nos. 11-12]**

State whether the device layer in any of the silicon on insulator products identified by Interrogatory Number 1, above, [1] contains a "predominant intrinsic point defect" at the center of the (circular) device layer as the quoted term is used in the Asserted Claims and, if not, explain in detail the factual basis for your belief and [2] identify all test results and documents which corroborate such belief.

**RESPONSE:**

Soitec objects to this interrogatory on the ground that, as posed, it is not susceptible of response because there can be no "predominant" species of defect "at the center" of a device layer, which is a point and therefore has no dimension. Soitec further objects to this interrogatory to the extent that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent it concerns products that MEMC has not accused of infringement in this lawsuit. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Soitec also objects that this interrogatory is vague and ambiguous to the extent it seeks an application of selected claim elements without providing MEMC's proposed construction of those elements. Soitec also objects to MEMC's

mischaracterization in this interrogatory of the scope and proper construction of the asserted claims in this lawsuit. Soitec further objects to this interrogatory as premature to the extent it seeks expert opinion prior to any scheduled exchange of expert reports.

To the extent that Soitec understands this interrogatory and subject to and without waiving the foregoing specific and general objections, and subject to amendment and modification pursuant to Fed. R. Civ. P. 26, Soitec preliminarily states that it is Soitec's present understanding that MEMC contends that it is an inherent property of a silicon crystal, however prepared, that it will have intrinsic point defects. Soitec does not dispute this contention insofar as it is intended to refer to the material constituting the device layer during the period or periods in the material's thermal and processing history when it is thermodynamically possible for intrinsic point defects to exist. Soitec specifically denies that such point defects exist in the device layers of the accused finished SOI products and denies that there is a predominant intrinsic point defect in the device layer of the finished SOI products. In corroboration of this contention, Soitec relies in part on the deposition testimony given in this case of Robert Falster, MEMC's Fed. R. Civ. P. 30(b)(6) designee and the named inventor on the '104 Patent, and will further rely on the report or reports of one or more of its expert witnesses and the materials cited therein in corroboration of this contention. Such reports will be submitted in conformity with the Court's scheduling order.

Further responding, Soitec states that, even accepting MEMC's contention to be true of the accused products, whether there is predominant type of intrinsic point defect in a device layer would depend on the processing history of the device layer. Further responding, Soitec states that it does not examine the device layers of its products to determine if the device layers "contains a 'predominant intrinsic point defect' at the center," is not aware of any means for

doing so, and has no reason to believe that the device layers of its products "contain[ ] a 'predominant intrinsic point defect' at the center," however understood..

Further responding, Soitec notes that MEMC appears to be contending that the limitations of the asserted claims covering a device layer "having . . . a predominant intrinsic point defect" should be interpreted to refer to a device layer which originates as part of a donor wafer which donor wafer has the claimed properties, regardless of whether the device layer retains the claimed properties when made, used, sold, or offered for sale in the United States or imported into the United States as part of the claimed silicon on insulator structure. Soitec denies that this is the proper interpretation of this limitation. Using (without adopting) MEMC's incorrect construction of this limitation, Soitec states that it is aware of testing purporting to determine whether its supplier's wafers have a first axially symmetric region in which there is a predominant intrinsic point defect only insofar as such testing has been performed by MEMC and only with respect to wafers supplied by SUMCO. Soitec further states, that such testing has been adjudicated not to be scientifically reliable, and that such wafers have been adjudicated to lack such a region. Soitec will further rely on the report or reports of one or more of its expert witnesses and the materials cited therein in corroboration of this contention. Such reports will be submitted in conformity with the Court's scheduling order.

Further responding, Soitec will contend that no known method has been developed to detect the presence of a silicon interstitial intrinsic point defect and that, as a consequence, there is no way to know in any silicon wafer whether interstitial or vacancy point defects are "predominant." Soitec will rely on the report or reports of one or more of its expert witnesses and the materials cited therein in corroboration of this contention. Such reports will be submitted in conformity with the Court's scheduling order.

**INTERROGATORY NO. 6: [Actual Interrogatory Nos. 13-14]**

State whether the device layer in any of the silicon on insulator products identified by Interrogatory Number 1, above, [1] contains "vacancies" as the "predominant intrinsic point defect" at the center of the (circular) device layer as the quoted terms are used in the Asserted Claims and, if not, explain in detail the factual basis for your belief and [2] identify all test results and documents which corroborate such belief.

**RESPONSE:**

Soitec objects to this interrogatory on the ground that, as posed, it is not susceptible of response because there can be no "predominant" species of defect "at the center" of a device layer, which is a point and therefore has no dimension. Soitec objects to this interrogatory to the extent that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent it concerns products that MEMC has not accused of infringement in this lawsuit. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Soitec also objects that this interrogatory is vague and ambiguous to the extent it seeks an application of selected claim elements without providing MEMC's proposed construction of those elements. Soitec also objects to MEMC's mischaracterization in this interrogatory of the scope and proper construction of the asserted claims in this lawsuit. Soitec further objects to this interrogatory as premature to the extent it seeks expert opinion prior to any scheduled exchange of expert reports.

To the extent that Soitec understands this interrogatory and subject to and without waiving the foregoing specific and general objections, and subject to amendment and modification pursuant to Fed. R. Civ. P. 26, Soitec preliminarily states that it is Soitec's present understanding that MEMC contends that it is an inherent property of a silicon crystal, however prepared, that it will have intrinsic point defects. Soitec does not dispute this contention insofar as it is intended to refer to the material constituting the device layer during the period or periods

in the material's thermal and processing history when it is thermodynamically possible for intrinsic point defects to exist. Soitec specifically denies that such point defects exist in the device layers of the accused finished SOI products and denies that there is a predominant intrinsic point defect in the device layer of the finished SOI products. Soitec will rely on the report or reports of one or more of its expert witnesses and the materials cited therein in corroboration of this contention. Such reports will be submitted in conformity with the Court's scheduling order.

Further responding, Soitec states that, even accepting MEMC's contention to be true of the accused products, whether there is predominant type of intrinsic point defect in a device layer depends on the processing history of the device layer.

Further responding, Soitec states that it does not examine the device layers of its products to determine if the device layers "contains 'vacancies' as the 'predominant intrinsic point defect' at the center," is not aware of any means for doing so, and has no reason to believe that vacancy point defects are predominant "at the center" (however understood) of the device layers of its wafers.

Further responding Soitec notes that MEMC has contended that the limitations of asserted claim 10 covering a device layer "wherein vacancies are the predominant intrinsic point defect within the first axially symmetric region comprising the central axis of the layer or having a width of at least about 15 mm, as measured along the radius of the layer" (which is presumably the limitation to which this interrogatory relates) should be interpreted to refer to a device layer which originates as part of wafer which source wafer has the claimed properties, regardless of whether the device layer retains the claimed properties when made, used, sold, or offered for sale in the United States or imported into the United States as part of the claimed

silicon on insulator structure. Soitec denies that this is the proper interpretation of this limitation. Using (without adopting) MEMC's incorrect construction of this limitation, Soitec states that it does not test the donor wafers from which its device layers are taken to determine whether the donor wafers have "'vacancies' as the 'predominant intrinsic point defect' at their center" and therefore lacks sufficient knowledge to respond further to this interrogatory at this time. Soitec further states that it is aware of testing purporting to determine whether its supplier's wafers have a first axially symmetric region in which vacancies are the predominant intrinsic point defect only insofar as such testing has been performed by MEMC and only with respect to wafers supplied by SUMCO. Soitec further states, that such testing has been adjudicated not to be scientifically reliable, and that such wafers have been adjudicated to lack such a region. Soitec will further rely on the report or reports of one or more of its expert witnesses and the materials cited therein in corroboration of this contention. Such reports will be submitted in conformity with the Court's scheduling order.

Further responding, Soitec will contend that no known method has been developed to detect the presence of a silicon interstitial intrinsic point defect and that, as a consequence, there is no way to know in any silicon wafer whether interstitial or vacancy point defects are "predominant." Soitec will rely on the report or reports of one or more of its expert witnesses and the materials cited therein in corroboration of this contention. Such reports will be submitted in conformity with the Court's scheduling order.

**INTERROGATORY NO. 7: [Actual Interrogatory Nos. 15-16]**

Separately for each Asserted Claim, state [1] how you construe each limitation of that claim which you believe to require construction; [2] the scope of equivalents under the doctrine of equivalents to which you contend the limitation is entitled; and the factual basis for your contentions.

**RESPONSE:**

Soitec objects to this interrogatory to the extent it seeks information or documents protected by the attorney-client privilege or work product immunity. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Soitec further objects to this interrogatory as premature to the extent it seeks expert opinion and claim construction contentions prior to any scheduled exchange of expert reports or claim construction contentions. Soitec further objects to this interrogatory to the extent that it requests the "scope of equivalents" for each limitation of the asserted claims as premature and beyond the scope of discovery. If and when MEMC accuses any Soitec product of meeting any limitation of the asserted claims under the doctrine of equivalents, Soitec will, subject to all of the foregoing objections, state whether it agrees or disagrees with any such contention and provide its factual basis for so doing.

Soitec does not know yet the identity of claim terms that will require construction because it has not had sufficient opportunity to determine whether MEMC interprets various terms in a different manner and lacks, among other things, the testing upon which MEMC purports to base its allegations of infringement. However, subject to and without waiving the foregoing specific and general objections, and subject to amendment and modification pursuant to Fed. R. Civ. P. 26, Local Rules and Standing Order, Soitec preliminarily states that the phrase "device layer" of an SOI wafer should be construed to mean, "the layer in a silicon on insulator substrate extending from the surface of the wafer to the top of the buried insulating layer" *e.g.*, '104 Patent, 1:22-26, 21:13-38, 14:34-37, 20:48-57; the phrase "intrinsic point defect" should be construed to mean "a vacancy defect or a self-interstitial defect," *e.g.*, *id.*, at 1:45-55; the phrase "axially symmetric" should be construed to mean "symmetric with respect to the central axis of

the device layer"; the term "region" should be construed to mean "an area of the wafer"; the phrase "a predominant intrinsic point defect" should be construed to mean "a type of intrinsic point defect that is the dominant type of intrinsic point defect" in a specified region *e.g., id.*, at 14:16-23, 15:40-56 and Figs. 13-14, 16:6-24, 19:59-20:2 and Fig. 15, 30:62-67, and 33:30-34 and Fig 33; and the phrase "agglomerated intrinsic point defects" should be construed to mean "defects caused (i) by the reaction during the formation of a single crystal silicon ingot in which vacancies agglomerate to produce D-defects, flow pattern defects, gate oxide integrity defects, crystal originated particle defects, crystal originated light point defects, and other such vacancy related defects, or (ii) by the reaction during the formation of a single crystal silicon ingot in which self-interstitials agglomerate to produce dislocation loops and networks, and other such self-interstitial related defects." '104 Patent 22:61-23:1. Further responding, Soitec states that the "definition" provided in the patent for the phrase "substantially free of agglomerated intrinsic point defects" is ambiguous and cannot be construed . '104 Patent at 23:8-12. Soitec states that it is continuing its investigation of the meaning of this phrase and will supplement this response in due course.

**INTERROGATORY NO. 8: [Actual Interrogatory Nos. 17-22]**

[1-3] Identify all prior art which you believe is relevant to the validity or enforceability of any of the Asserted Claims; and [4-6] identify with particularity where you believe any limitation of an Asserted Claim is found in any of such prior art.

**RESPONSE:**

Soitec objects to this interrogatory in that the request to identify "all prior art . . . relevant to the validity or enforceability of any of the Asserted Claims" seeks information or documents protected by the attorney-client privilege or work product immunity. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Soitec objects that the interrogatory is also premature because it seeks

expert opinion prior to any scheduled exchange of expert reports. Soitec further objects that this interrogatory is unduly burdensome and purports to impose obligations on Soitec in excess of those allowed under the Federal Rules of Civil Procedure. Soitec also objects that this interrogatory is premature because Soitec has not completed discovery on the information sought by this interrogatory. Soitec objects that the interrogatory is also premature because MEMC has to date failed to provide Soitec with MEMC's proposed claim constructions and the Court has not yet construed the asserted claims.

Subject to and without waiving the foregoing specific and general objections, Soitec states that such prior art includes at least the art identified on the face of the '104 Patent, the art cited to and considered by the US and European Patent Offices in connection with related applications (including applications relating to MEMC's so-called perfect silicon and magic denuded zone technologies), the art disclosed by SUMCO in its US litigation with MEMC and in its European opposition to MEMC's patents. To the extent that additional art exists and Soitec possesses it, Soitec has produced such prior art, including documents memorializing Soitec's own conception and reduction to practice of the claimed inventions.. Soitec further states that each asserted claims is invalid for failure to meet the conditions of patentability set forth in 35 U.S.C. §§ 102 and 103. Charts indicating which references disclose which limitations are attached to these interrogatories as Exhibit A. Further, such information was provided by the examiner in U.S. Patent Application 10/963,137 (now abandoned) in his non-final rejection of January 31, 2007, with respect to subject matter deemed by the examiner to be substantially identical to the subject matter of the claims at issue.

**INTERROGATORY NO. 9: [Actual Interrogatory No. 23-25]**

State whether you consider it obvious to combine any prior art to render any of the Asserted Claims invalid and, if so, explain where you find any teaching in the prior art to combine such prior art references.

**RESPONSE:**

Soitec objects to Interrogatory No. 9 insofar as it requests identification of a "teaching in the prior art to combine . . . prior art references" which is not the relevant legal standard. Further responding, Soitec contends that such combinations include at least the combinations cited by the examiner in U.S. Patent Application 10/963,137 (now abandoned) in his non-final rejection of January 31, 2007, with respect to subject matter deemed by the examiner to be substantially identical to the subject matter of the claims at issue. Further responding, see Soitec's response to Interrogatory No. 8 and Exhibit A.

**INTERROGATORY NO. 10: [Actual Interrogatory Nos. 25-42]**

Separately for each Asserted Claim, describe in detail the applicability of each of the secondary considerations of non-obviousness as set forth in *Graham v. John Deere*, 383 U.S. 1 (1966) and its progeny to the Asserted Claim.

**RESPONSE:**

Soitec objects to this interrogatory to the extent it seeks information or documents protected by the attorney-client privilege or work product immunity. Soitec objects that the interrogatory is also premature because it seeks expert opinion prior to any scheduled exchange of expert reports. Soitec further objects that this interrogatory is unduly burdensome and purports to impose obligations on Soitec in excess of those allowed under the Federal Rules of Civil Procedure. Soitec also objects that this interrogatory is premature because Soitec has not completed discovery on the information sought by this interrogatory; Soitec reserves the right to supplement its response to this interrogatory after it has completed such discovery. Soitec has

not received any of MEMC's documents or things in discovery in this litigation, nor has Soitec conducted any depositions of MEMC's witnesses. Soitec has not received discovery concerning the licensing history of the patent-in-suit.

Subject to and without waiving the foregoing specific and general objections, Soitec states the following:

(a) Commercial Success: To date, MEMC has not provided any documentation showing that it has succeeded in manufacturing SOI products that embody or embodied the Asserted Claims. Rather, the discovery produced by MEMC shows that it has been unable to produce SOI products that embody the Asserted Claims and has completely failed to achieve any commercial success by practicing the claimed invention. Soitec's commercial success for its SOI products is due to its Smart Cut® technology and has no basis in any asserted use of subject matter related to the asserted claims.

(b) Long Felt Need: The commercial failure of MEMC's SOI products embodying the invention is indicative of the absence of a long felt need. Further, though the patent recites that "a need continues to exist for a SOI substrate which contains a device layer which is substantially free of agglomerated intrinsic point defects," the existence of SOI with "no COPS" device layers dates back at least to the 1980's. Hence, the patent does not address a long felt need. Further, within months of the publication of research identifying a potential connection between certain HF defects and the presence of COPS in device layer starting material, Soitec was able to manufacture SOI using low and/or no COPS starting material for the device layer. Soitec had commercialized such products before the named inventor of the '104 patent had reduced his alleged invention to practice.

(c) Failed Efforts of Others: Others who sought to address the "problem" supposedly resolved by the '104 Patent did not fail in their efforts to do so. Rather, Soitec and others successfully produced SOI with a device layer substantially free of agglomerated point defects (as that phrase as appears to have been used by MEMC in connection with its allegation that Soitec has infringed the '104 Patent) before MEMC did.

(d) Success in Licensing: Soitec is informed and believes that MEMC has had no success in licensing the '104 patent.

(e) Copying: Soitec and others did not copy MEMC's SOI wafers. Rather, Soitec and others were producing SOI wafers with a device layer substantially free of agglomerated point defects, (as that phrase as appears to have been used by MEMC in connection with its allegation that Soitec has infringed the '104 Patent), before MEMC filed its application for the '104 patent and long before MEMC produced any such SOI wafers.

(f) Independent Invention: Soitec and others produced SOI with a device layer substantially free of agglomerated point defects (as that phrase as appears to have been used by MEMC in connection with its allegation that Soitec has infringed the '104 Patent) before MEMC did.

**INTERROGATORY NO. 11: [Actual Interrogatory Nos. 43-44]**

Describe in detail all methods by which you contend it is possible to determine whether [1] there is a predominant intrinsic point defect and/or [2] a region that is substantially free of agglomerated intrinsic point defects in the device layer of any of the products identified by Interrogatory Number 1, above.

**RESPONSE:**

Soitec objects to this interrogatory to the extent that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent it concerns products that MEMC has not accused of

infringement in this lawsuit. Soitec also objects to this interrogatory to the extent it is duplicative of Interrogatory Nos. 4 and/or 5. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Soitec also objects that this interrogatory is vague and ambiguous to the extent it seeks an application of selected claim elements without providing MEMC's proposed construction of those elements. Soitec also objects to MEMC's mischaracterization in this interrogatory of the scope and proper construction of the asserted claims in this lawsuit.

Subject to and without waiving the foregoing specific and general objections, Soitec states that it is unaware of any method to determine whether there is a predominant intrinsic point defect and/or a region that is substantially free of agglomerated intrinsic point defects in the device layer of any of the products identified by Interrogatory Number 1 and believes that no such method exists. Further, due to the ambiguity of the claim language, Soitec is uncertain as to what would count as a scientifically reliable test to determine that "agglomerated intrinsic point defects" are "substantially absent" from a device layer as those terms are used in the asserted claims.

**INTERROGATORY NO. 12: [Actual Interrogatory Nos. 45-46]**

State the [1] circumstances under which you first learned of the '104 patent; [2] identify all persons with knowledge of such circumstances; and state the time frame when the circumstances occurred.

**RESPONSE:**

Soitec objects to this interrogatory to the extent it seeks information or documents protected by the attorney-client privilege or work product immunity. Soitec objects to this interrogatory on the grounds that it is unduly burdensome and vague. Soitec objects to this interrogatory to the extent it seeks information that is irrelevant to any claim or defense in this

action. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory.

Subject to and without waiving the foregoing specific and general objections, Soitec states that it learned that MEMC contended that Soitec infringed one or more claims of the '104 patent on receipt of a letter dated October 15, 2004, which, on information and belief, was sent by Dr. Shaker Sadasivam of MEMC to Mr. Emmanuel Huyghe of Soitec. A true and correct copy of that letter was attached as Exhibit 1 to Soitec's Complaint in this case.

**INTERROGATORY NO. 13: [Actual Interrogatory No. 47]**

State the substance of any opinion (oral or written) which Soitec has ever received concerning the validity, infringement or enforceability of the '104 patent and, for each such opinion, identify the date the opinion was given, the person(s) who gave the opinion, and the person(s) who heard or received the opinion.

**RESPONSE:**

Soitec objects to this interrogatory to the extent it seeks information or documents protected by the attorney-client privilege or work product immunity.

Subject to and without waiving the foregoing specific and general objections, Soitec states that pursuant to Fed. R. Civ. P. 33(d), Soitec has produced non-privileged documents and has logged privileged documents.

**INTERROGATORY NO. 14: [Actual Interrogatory Nos. 48-49]**

With respect to each prior art silicon on insulator product which you believe invalidates any or all of the Asserted Claims, [1] identify all starting materials used in making the product; [2] describe each step of the process whereby each such product was made; and describe all conditions under which each step was performed.

**RESPONSE:**

Soitec objects to this interrogatory to the extent it seeks information or documents protected by the attorney-client privilege or work product immunity. Soitec also objects to this

interrogatory to the extent it is duplicative of Interrogatory No. 8. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Soitec objects that the interrogatory is also premature because it seeks expert opinion prior to any scheduled exchange of expert reports. Soitec further objects that this interrogatory is unduly burdensome and purports to impose obligations on Soitec in excess of those allowed under the Federal Rules of Civil Procedure. Soitec also objects that this interrogatory is premature because Soitec has not completed discovery on the information sought by this interrogatory; Soitec reserves the right to supplement its response to this interrogatory after it has completed such discovery. Soitec objects that the interrogatory is also premature because MEMC has to date failed to provide Soitec with MEMC's proposed claim constructions and the Court has not yet construed the asserted claims.

Subject to and without waiving the foregoing specific and general objections, Soitec states that pursuant to Fed. R. Civ. P. 30(b)(6) and 33(d), Soitec has produced witnesses and non-privileged documents from whom and from which MEMC can identify prior art silicon on insulator products and the starting materials and process steps used in their manufacture. Further responding, see responses to Interrogatories 8 and 9 and Exhibit A.

**INTERROGATORY NO. 15: [Actual Interrogatory Nos. 50-51]**

[1] Identify all starting materials and [2] describe each step of the process whereby Soitec makes each of the products identified by Interrogatory Number 1, and describe all conditions under which each step is performed.

**RESPONSE:**

Soitec objects to this interrogatory on the grounds that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent it concerns products that MEMC has not accused of infringement in this lawsuit. Soitec also objects that this interrogatory comprises numerous

unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Soitec also objects that this interrogatory is vague and ambiguous to the extent it seeks an application of selected claim elements without providing MEMC's proposed construction of those elements. Soitec also objects to MEMC's mischaracterization in this interrogatory of the scope and proper construction of the asserted claims in this lawsuit.

Subject to and without waiving the foregoing specific and general objections, Soitec states that pursuant to Fed. R. Civ. P. 30(b)(6) and 33(d), Soitec has produced witnesses and non-privileged documents from which MEMC can identify the starting materials and the principal process steps used in their manufacture of the products identified in Soitec's response to Interrogatory Number 1.

**INTERROGATORY NO. 16: [Actual Interrogatory Nos. 52-53]**

[1] Describe in detail the factual basis for your contentions in Paragraph 28 of the (Corrected) First Amended Complaint for Declaratory Judgment and [2] identify all witnesses with knowledge of such purported facts.

**RESPONSE:**

Soitec objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory.

Subject to and without waiving the foregoing specific and general objections, Soitec states that HF defects were first identified in SOI device layers in a paper presented by D.K. Sadana, et al. at the IEEE International SOI Conference in October 1994. The paper was titled "Nano-Defects in Commercial Bonded SOI and SIMOX." Various theories were offered to explain HF defects, including the possibility that such defects were caused by oxygen precipitates, by the oxidation of the device layer, or by grown in defects in the starting material from which the device layer was taken.

Soitec began a project known as "JESSI" in cooperation with LETI and Wacker to determine, among other things, the relationship between the quality of starting material (including its agglomerated intrinsic point defects, as measured by various general techniques for detecting defects that would be included among "agglomerated intrinsic point defects"). The results of this project were publicly presented, in part, by André-Jacques Auberton-Hervé in 1996 (see below).

"COP defects" [by that name] were definitively identified as grown in defects in August 1996 in a paper presented by Takemi Ueki, et al. at the International Conference on Solid States Devices and Materials. The paper was titled "Octahedral Void Structure Observed at the Grown-In Defects in the Bulk of Standard CZ-Si for MOSLIs." An association between COP defects and the breakdown of a wafer's gate oxide integrity was demonstrated in a paper by D. Graf, et al. at the Fall 1996 Meeting of the Electro-Chemical Society, and the association between HF defects in SOI device layers and grown in COP defects in the starting material from which the device layers were taken was disclosed at the December 1996 IEDM Conference in a presentation by André-Jacques Auberton-Hervé of Soitec titled "SOI: Materials to Systems." Witnesses with knowledge of these facts include the authors of these papers and presentations.

**INTERROGATORY NO. 17: [Actual Interrogatory Nos. 54-55]**

[1] Describe in detail the factual basis for your contentions in Paragraph 33 of the (Corrected) First Amended Complaint for Declaratory Judgment and [2] identify all witnesses with knowledge of such purported facts.

**RESPONSE:**

Soitec objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory.

Subject to and without waiving the foregoing specific and general objections, Soitec states that pursuant to Fed. R. Civ. P. 30(b)(6) and 33(d), Soitec has produced witnesses and

documents sufficient to describe the factual basis for the allegations of Paragraph 33 of the First Amended Complaint and persons with knowledge thereof.

**INTERROGATORY NO. 18: [Actual Interrogatory Nos. 56-57]**

[1] Describe in detail the factual basis for your contentions in Paragraph 34 of the (Corrected) First Amended Complaint for Declaratory Judgment and [2] identify all witnesses with knowledge of such purported facts.

**RESPONSE:**

Soitec objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory.

Subject to and without waiving the foregoing specific and general objections, Soitec states that pursuant to Fed. R. Civ. P. 30(b)(6) and 33(d), Soitec has produced witnesses and produce documents sufficient to describe the factual basis for the allegations of Paragraph 34 of the First Amended Complaint and persons with knowledge thereof.

**INTERROGATORY NO. 19: [Actual Interrogatory Nos. 58-59]**

[1] Describe in detail the factual basis for your contentions in Paragraph 38(c) of the (Corrected) First Amended Complaint for Declaratory Judgment that "...the Prior Art Silicon produced by these techniques was substantially identical to the silicon (the "MEMC Silicon") produced by the technique (the "MEMC Technique") purportedly disclosed in the '302 and the '104 Patents"; and [2] identify all witnesses with knowledge of such purported facts.

**RESPONSE:**

Soitec objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory.

Subject to and without waiving the foregoing specific and general objections, Soitec states that the disclosure of the '302 patent (though not the disclosure of the '104 patent) acknowledges such substantial identity, *e.g.*, '302 Patent, at 2:37-3:7, as did the specifications of multiple other patents assigned to MEMC and SiBond which have been or will be marked as deposition exhibits in this case. Witnesses with knowledge of such facts include the named

inventors on, and persons who prepared and prosecuted these patents. Further responding, see references discussed in Exhibit A. Further responding, Soitec and MEMC have produced MEMC sales presentations made to Soitec and other MEMC promotional materials acknowledging the substantial identity of its epitaxial, annealed, "low COP", and "COP free" products.

**INTERROGATORY NO. 20: [Actual Interrogatory No. 60]**

If you contend there are any industry standard royalty rates applicable to the '104 patent or any product accused of infringement thereunder, then please describe such royalty rates, and state the factual basis for your contentions.

**RESPONSE:**

Soitec objects to the phrases "industry standard" and "applicable to the '104 patent or any product accused of infringement thereunder" as vague and ambiguous.

Soitec further objects that this interrogatory is premature because Soitec has not completed, and MEMC has failed to provide, discovery on the information sought by this interrogatory and because MEMC has to date failed to provide Soitec with any information regarding MEMC's damages claims. Soitec reserves the right to supplement its response to this interrogatory after it has completed such discovery. Soitec further objects to this interrogatory to the extent it seeks expert opinion prior to any scheduled exchange of expert reports.

**INTERROGATORY NO. 21: [Actual Interrogatory No. 61]**

Identify all persons responsible for selling or promoting any product identified by Interrogatory Number 1, above, and summarize the responsibilities of each identified person.

**RESPONSE:**

Soitec objects to this interrogatory on the grounds that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent it concerns products that MEMC has not accused of

infringement in this lawsuit. Soitec also objects that this interrogatory is vague and ambiguous to the extent it seeks an application of selected claim elements without providing MEMC's proposed construction of those elements. Soitec also objects to MEMC's mischaracterization in this interrogatory of the scope and proper construction of the asserted claims in this lawsuit.

Subject to and without waiving the foregoing specific and general objections, Soitec states that person responsible for selling or promoting the products identified by the response to Interrogatory Number 1 is Michael Wolf, Senior Vice President, Marketing and Sales. Pursuant to Fed. R. Civ. P. 30(b)(6) and 33(d), Soitec has produced witnesses and non-privileged documents from whom and from which MEMC can determine the responsibilities of each identified person and the identity of other persons, if any, responsible for selling or promoting the products identified by the response to Interrogatory Number 1.

**INTERROGATORY NO. 22: [Actual Interrogatory No. 62]**

Identify all subsidiaries, divisions, parents, joint venturers, or any other commercial entity involved in the manufacture, distribution or sale of any of the products identified by Interrogatory Number 1, above, and summarize the nature of such involvement.

**RESPONSE:**

Soitec incorporates by reference its objections to Interrogatory Number 1. Soitec further objects to this interrogatory on the grounds that it is vague, ambiguous, overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence.

Subject to and without waiving the foregoing specific and general objections, Soitec states that S.O.I.TEC Silicon on Insulator Technologies S.A. is involved in the manufacture of the products identified in its response to Interrogatory Number 1, and Soitec U.S.A., Inc. is involved in the distribution and sale of the products identified in its response to Interrogatory Number 1 in the United States.

**INTERROGATORY NO. 23: [Actual Interrogatory Nos. 63-64]**

State the [1] gross U.S. sales per month or quarter in units and in currency for each of the products identified by Interrogatory Number 1, above, during the period from May 22, 2001 to present; [2] identify the amount of gross and net profit attributable to sales of each such product; and explain how such profits are calculated.

**RESPONSE:**

Soitec incorporates by reference its objections to Interrogatory Number 1. Soitec further objects to this interrogatory on the grounds that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent it concerns products that MEMC has not accused of infringement in this lawsuit.

Subject to and without waiving the foregoing specific and general objections, Soitec states that pursuant to Fed. R. Civ. P. 30(b)(6) and 33(d), Soitec has produced or will produce witnesses and has produced non-privileged documents from which MEMC can determine Soitec's U.S. sales of the products identified in the response to Interrogatory Number 1 during the relevant time period (in units and currency), and its gross and net profits from those sales.

**INTERROGATORY NO. 24: [Actual Interrogatory No. 65]**

State whether Soitec ever performs a "flow pattern defect" test on silicon using an etchant and, if so, please describe each step of the test and explain all conditions under which the test is performed.

**RESPONSE:**

Soitec objects to this interrogatory to the extent it seeks information or documents protected by the attorney-client privilege or work product immunity. Soitec further objects to this interrogatory on the grounds that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent that it is irrelevant to the Asserted Claims and/or concerns products that MEMC has not

accused of infringement in this lawsuit. Soitec also objects that the term "silicon" is vague and ambiguous rendering much of this interrogatory incomprehensible.

To the extent that Soitec understands this interrogatory and subject to and without waiving the foregoing specific and general objections, Soitec states that it does not currently, and has not ever on a routine basis, performed a "flow pattern defect" test.

Subject to and without waiving the foregoing specific and general objections, Soitec states that pursuant to Fed. R. Civ. P. 30(b)(6) and 33(d), Soitec has produced witnesses and available non-privileged documents from whom and from which MEMC can determine any "flow pattern defect" test.

**INTERROGATORY NO. 25: [Actual Interrogatory No. 66]**

State whether Soitec ever performs a "bulk microdefect" test on silicon and, if so, please describe each step of the test and explain all conditions under which the test is performed.

**RESPONSE:**

Soitec objects to this interrogatory to the extent it seeks information or documents protected by the attorney-client privilege or work product immunity. Soitec further objects to this interrogatory on the grounds that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent that it is irrelevant to the Asserted Claims and/or concerns products that MEMC has not accused of infringement in this lawsuit. Soitec also objects that the term "silicon" is vague and ambiguous rendering much of this interrogatory incomprehensible.

To the extent that Soitec understands this interrogatory and subject to and without waiving the foregoing specific and general objections, Soitec states that it does perform a "bulk microdefect" test on handle wafers and, pursuant to Fed. R. Civ. P. 30(b)(6) and 33(d), Soitec

has produced witnesses and non-privileged documents from whom and from which MEMC can determine the steps of the test and the conditions under which the test is performed.

**INTERROGATORY NO. 26: [Actual Interrogatory No. 67]**

State whether Soitec ever performs a test for oxygen precipitation on silicon and, if so, please describe each step of the test and explain all conditions under which the test is performed.

**RESPONSE:**

Soitec objects to this interrogatory to the extent it seeks information or documents protected by the attorney-client privilege or work product immunity. Soitec further objects to this interrogatory on the grounds that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent that it is irrelevant to the Asserted Claims and/or concerns products that MEMC has not accused of infringement in this lawsuit. Soitec also objects that the term "silicon" is vague and ambiguous in this interrogatory rendering much of this interrogatory incomprehensible.

To the extent that Soitec understands this interrogatory and subject to and without waiving the foregoing specific and general objections, Soitec states that it does perform a test for oxygen precipitation on bulk silicon and, pursuant to Fed. R. Civ. P. 30(b)(6) and 33(d), Soitec has produced witnesses and available non-privileged documents from whom and from which MEMC can determine the steps of the test and the conditions under which the test is performed.

**INTERROGATORY NO. 27: [Actual Interrogatory No. 67]**

Describe in detail all tests performed by or at the direction of Soitec on any silicon on insulator products or raw materials used in making same.

**RESPONSE:**

Soitec objects to this interrogatory to the extent it seeks information or documents protected by the attorney-client privilege or work product immunity. Soitec further objects to

this interrogatory to the extent that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent it concerns products that MEMC has not accused of infringement in this lawsuit. Soitec also objects that the phrases "any silicon on insulator products" and "raw materials" are vague and ambiguous rendering much of this interrogatory incomprehensible.

Soitec states that it does perform various tests on bulk silicon and, pursuant to Fed. R. Civ. P. 30(b)(6) and 33(d), Soitec has produced witnesses and available non-privileged documents from whom and from which MEMC can determine the steps of the test and the conditions under which the test is performed.

**INTERROGATORY NO. 28: [Actual Interrogatory Nos. 68-70]**

Are the wafers made by [1] SEH, [2] SUMCO and [3] Siltronic which were seized (per the French laws) by MEMC from your facility in December 2005 representative of donor wafers you have historically received from SEH, SUMCO and Siltronic under Bulk Codes SO-1308-SEH, 50-1309-SUM and SO-1371-SIL, respectively, for use in making SOI products and, if not, state all reasons why such wafers are not representative of such respective larger groups of wafers.

**RESPONSE:**

Soitec further objects to this interrogatory on the grounds that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent it concerns products that MEMC has not accused of infringement in this lawsuit. Soitec also objects that the term "representative" and phrase "historically received" are vague and ambiguous rendering much of this interrogatory incomprehensible.

To the extent that Soitec understands this interrogatory and subject to and without waiving the foregoing specific and general objections, Soitec states that the seized SEH, SUMCO, and Siltronic wafers were represented by SEH, SUMCO, and Siltronic to be

representative of donor wafers that Soitec received from SEH, SUMCO, and Siltronic in the regular course of business before the inception of the instant lawsuit. Soitec cannot and does not confirm this representation.

**INTERROGATORY NO. 29: [Actual Interrogatory Nos. 71-72]**

[1] Identify each of your silicon on insulator products by name and product number which was made using a "COP free" wafer for the handle and which was made, used, offered for sale, sold or shipped into the United States since May 22, 2001, and [2] identify the customer for each of those products.

**RESPONSE:**

Soitec objects to this interrogatory to the extent that it is overly broad, unduly burdensome, and seeks information not reasonably calculated to lead to the discovery of admissible evidence to the extent it concerns products that MEMC has not accused of infringement in this lawsuit. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Because of the number of unrelated sub-parts in this interrogatory and MEMC's other interrogatories, MEMC has exceeded the number of interrogatories allowed under Local Rule 26.1(b). Soitec also objects that this interrogatory is vague and ambiguous to the extent it seeks an application of selected claim elements without providing MEMC's proposed construction of those elements. Soitec also objects to MEMC's mischaracterization in this interrogatory of the scope and proper construction of the asserted claims in this lawsuit.

Subject to and without waiving the foregoing specific and general objections, Soitec states that none of its silicon on insulator products were made using a "COP free" wafer for the handle and were made, used, offered for sale, sold or shipped into the United States since at least May 22, 2001.

**INTERROGATORY NO. 30: [Actual Interrogatory Nos. 73-74]**

If Soitec intends to offer or to introduce any evidence, including, but not limited to, documents, objects, devices, or software (in any form, including source code and/or object code form), or the testimony of any witnesses [1] at the tutorial describing the technology and matters in issue or [2] at the hearing on claim construction in this matter, identify any such evidence and each such witness, and for each witness set forth in detail the testimony that Soitec anticipates he or she will provide at the tutorial and/or hearing.

**RESPONSE:**

Soitec objects to this interrogatory to the extent it seeks information or documents protected by the attorney-client privilege or work product immunity. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Because of the number of unrelated sub-parts in this interrogatory and MEMC's other interrogatories, MEMC has exceeded the number of interrogatories allowed under Local Rule 26.1(b). Soitec further objects to this interrogatory to the extent it seeks expert opinion prior to any scheduled exchange of expert reports. Soitec also objects that this interrogatory is premature in that Soitec has not yet decided which evidence, witnesses and/or testimony it will use for the tutorial and/or hearing.

**INTERROGATORY NO. 31: [Actual Interrogatory Nos. 75-77]**

Identify each source of information that you considered in preparing your responses to these interrogatories including, but not limited to, [1] all persons who provided information that you considered in preparing your responses, [2] all persons who you interviewed in connection with gathering information sought in these interrogatories, and [3] all documents that you reviewed for purposed [sic] of gathering information sought in these interrogatories.

**RESPONSE:**

Soitec objects to this interrogatory to the extent it seeks information or documents protected by the attorney-client privilege or work product immunity. Soitec also objects that this interrogatory comprises numerous unrelated sub-parts, each of which is considered and counts as a separate interrogatory. Because of the number of unrelated sub-parts in this interrogatory and

MEMC's other interrogatories, MEMC has exceeded the number of interrogatories allowed under Local Rule 26.1(b).

Dated: January 2, 2008

EDWARDS ANGELL PALMER & DODGE LLP

*/s/Denise Seastone Kraft*

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## CERTIFICATE OF SERVICE

The undersigned hereby certifies that on January 2, 2008, a true and correct copy of the foregoing **Soitec's Supplemental and Amended Responses to MEMC's First Set of Interrogatories (Nos. 1-31)** was served upon the following counsel of record in the manner indicated.

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